Question Bank (K Scheme)

Name Of Subject: VLSI APPLICATIONS **Unit Test: I**

Subject Code: 316340 **Course: EJ6K**

Semester: VI

Chapter 1: Introduction TO CMOS technology **14 M**

2 Marks

1) State the important application of VLSI.
2) List the basics IC fabrication process
3)Define: a) Metastability
b)Noise Margin c) Power Dissipation d) Fan-Out e)skew

4 Marks

4) Comparison between BJT & CMOS.
5) Explain with neat diagram wafer processing by C-Z method.
6) Explain CMOS as a transmission gate.
7) Explain n well fabrication process of CMOS.
8) Explain the Twin tub process for fabrication of IC
9) Explain operation of CMOS NOR gate
10) Explain operation of CMOS NAND gate.
11) Design a logic circuit for $Z = \overline{AB + CD}$ using CMOS NAND gate.

Chapter 2: Advance Programmable Digital Devices (CPLD, FPGA, ASIC) **10 M**

2 Marks

1) Comparison between Melay & Moore machines.
2) List and explain feature of CPLD.
3) Explain feature of FPGA.
4) State the applications of CPLD and FPGA.

4 Marks

5) Differentiate between asynchronous sequential and synchronous sequential circuits.
6) Draw & explain Melay machines.
7) Draw & explain Moore machines.

8) Draw state diagram & block diagram of Melay state machine with clocked output.
9) Draw state diagram & block diagram of Moore state machine with clocked output.
10) Explain 3-bit asynchronous down counter.
11) Design a sequence detector to detect the sequence 011 using JK flip flop. Use Mealy machine
12) Draw and Explain block diagram of CPLD architecture.
13) Draw and Explain block diagram of FPGA architecture.
14) Draw & explain ASIC Design flow.
15) Differentiate between FPGA and CPLD

Unit - III Introduction to VLSI Design Concepts **16 Marks**

2 Marks

1) Define:
a)Entity b)Architecture c) Configuration d)package e) library
2) What is the difference between VHDL and Verilog?

3) List any two arithmetic operators in VHDL.

4) List any two logical operators in VHDL.

4 Marks

5)State the use and syntax of a)Signal b)Variable c) Constant
6) Compare VHDL and Verilog
7) Explain entity and architecture with an example.
8) Explain VHDL data types with examples.
9) Differentiate between signal and variable.
10)Explain the different VHDL objects: signal, variable, and constant.
11)Explain enumerated data types and their applications