QUESTION BANK
(K-Scheme)

Name of subject: Digital Techniques
Course Title: DTE (313303) **Unit Test: I**
Semester: 3K **Program Code: CM/EJ**

CHAPTER 1: Number Systems

2 marks

1. Write the base of the following number systems: Decimal, Binary, Octal, and Hexadecimal.
2. Give two applications of EX-OR and EX-NOR gates each.
3. List the binary, octal and hexadecimal numbers for decimal no. 0 to 15
4. Draw the logical symbol of EX-OR and EX-NOR gate.
5. Convert the following binary number (11001101)2 into Gray Code and Excess-3 Code.
6. Define 1's and 2's Complement of Binary Number with example.
7. Define 9's and 10's Complement of Binary Number with example.
8. Convert the following Binary number into Gray code.

(i) 1111
(ii) 1101001

4 marks

1. Convert the following:

i)(5C7)16=(?)10
ii)(2598)10 = (?)16
iii)(10110)2 = (?)10 = (?)16

2. Perform the following subtraction using 1's and 2's complement method:
i)(52)10 – (65)10
ii)(101011)2 – (11010)2

3. Perform the following subtraction
(i)Perform the BCD Addition. (17)10 + (57)10
(ii)Perform the binary addition. (10110.110)2 + (1001.10)2

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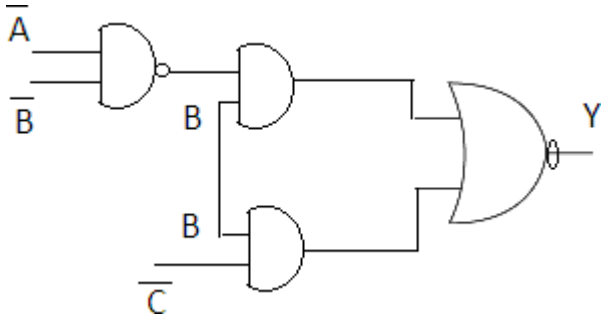
CHAPTER 2: Logic Gates and Boolean Algebra

2 marks

1. Define following characteristics of logic families :
    a. Propagation Delay
    b. Noise Margin
2. State commutative and associative laws for the binary numbers.
3. Define fan-in and fan-out of a gate.
4. Draw the Symbol and write the Truth Table of Universal Gates.

4 marks

1. For the given figure No. 1, derive the Boolean expression of Y.



1. Figure No. 1

2. Realize the following logic operations AND and OR using NAND and NOR gates only
3. Compare TTL and CMOS logic families on the basis of following:
    a. Propagation delay
    b. Power dissipation
    c. Speed of operation
    d. Basic gates
4. State and prove De Morgan's Theorems.
5. Reduce the following Boolean expression using Boolean laws.

$$Y=AB+\overline{A}B+A\overline{B}+\overline{AB}$$

6. Design EX-OR and EX-NOR gates using NAND and NOR gate.

CHAPTER 3: Combinational Logic Circuits

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2 marks

1. Draw three variable K-map formats.
2. State the necessity of multiplexer.
3. Draw Block diagram of 4:1 Multiplexer and write its truth table.
4. Identify function of following ICs. (i) 74244(ii) 74245.
5. Write simple example of Boolean expression for SOP and POS.
6. Draw two variable K-map format.

4 marks

1. M

inimize the following expression using K-map.

F (P, Q, R, S) = Σ m (0, 1, 4, 5, 7, 8, 9, 12, 13, 15).

2. Simplify the following Boolean Expression and Implement using logic gate.
   $A\bar{B} + A\bar{B}D + ABC\bar{} + ABCD$
3. Describe the function of Half Substractor Circuit using its truth table, K-Map simplification and logic diagram.
4. Describe the function of full Adder Circuit using its truth table, K-Map simplification and logic diagram.
5. Design BCD Adder using IC 7483
6. Reduce the following expression using K-map and implement it.
   a. F(A,B,C,D) = M (1,3,5,7,8,10,14)
7. Design Gray to Binary converter.
8. Draw the circuit diagram of BCD to 7 segment decoder and write its truth table.
9. Give the function of the following terminals of IC 7447.
   a. LT ii) RBI iii) BI iv) RBO
10. Realize the following function using:

I)F1 = Σ m (1, 2, 5, 6, 7,11)

II)F2 = π M (0, 1, 2, 5, 6, 7, 8, 11, 12, 15)