Question Bank (G scheme)

Name of subject: Principles of Digital Techniques

Subject code: 17320 **Unit Test: II**

Semester: III **Course: EJ/IS/IE**

Chapter.3: Combinational Logic Circuit (14 Marks)

3 marks

1) Implement the following using MUX
   a. $Y=\Sigma$ m (2, 3, 5, 6)

2) Give advantage of MUX.
3) Differentiate between MUX & DEMUX
4) What is Tristate buffer? Draw its symbol & IC NO.

4 marks

5) What is Decoder? How Demux act as a Decoder.
6) Draw ckt dig of 1:4 Demux using logic gate.
7) Draw functional diagram &logic diagram of half adder with truth table

Chapter.4: Sequential Logic Circuit (24 Marks)

3 marks

8) Draw RS latch using NAND gate & write truth table.
9) Explain the use of Preset & Clear terminal of F/F.
10) Write the excitation table for D & T F/F
11) Draw block diagram of IC 7490.

4 marks

12) Differentiate between Sequential Logic & Combinational Logic.
13) Draw 3 bit Asynchronous down counter write truth table.
14) What is Race around condition & how it is eliminated?
15) Draw & explain SISO shift register.
16) Explain with diagram 3 bit ring counter using D F/F

Chapter.5: Data Converter (16 Marks)

3 marks

17) What is the necessity of Data converter? Write the types of data converter
18) Compare R-2R & binary weighted register (Any 3 points).
19) Define.
   a. Accuracy

b. Resolution
c. Conversion time

4 marks

20) Draw ckt for 3 bit binary weighted DAC.
21) Draw & Explain Successive approximation ADC.
22) Calculate Analog o/p of 4 bit DAC & digital i/p is 1011 Assume Vfs =5v.

Chapter.6: Memories (10 marks)

3 marks

23) Define memory? Write down types of memory.

4 marks

24) Draw static RAM cell (TTL) .Explain its operation.
25) Write difference between EPROM & Flash Memory.