Question Bank (G Scheme)

Name Of Subject: VLS **Unit Test: II**

Subject Code: 17659 **Course: EJ6G**

Semester: VI

Chapter 3: Introduction to VHDL 06 M

3 Marks

1) Define with example, the following terms related to VHDL
   a) Entity b) Architecture
   c) Configuration d) package

2) Explain different types of operators in VHDL.

4 Marks

3) List and explain the data types used in HDL.

Chapter 4: VHLD Programming 16M

3 Marks

4) Explain Data flow types modeling with an example.
5) What do you mean by testbench in VHDL design.
6) Explain process statement with example.

4 Marks

7) Compare data flow ,behavioral and structural modeling.
8) Write the VHDL code to implement the 8:1multiplexer logic.
9) Write a VHDL code for 3:8 decoder.
10) Write 4:1 MUX code in VDHL Using case statement.
11) Write VHDL code for 8:3 encoder.
12) Write VDHL code for JK fllipflop.

Chapter 5: HDL Simulation AND Synthesis 20 M

3 Marks

13) Write short note on event scheduling.
14) Explain simulation cycle.

4 Marks

15) Compare software and hardware description language.
16) Compare event- based simulator and cycled-based simulator.
17) Explain the concept of delta delay's.
18) Explain HDL design flow for synthesis.
19) What is the synthesis? Explain synthesis issues in brief.
20) Explain efficient coding styles rules.

Chapter 6: Introduction To ASIC, EPGA, PLD 16 M

3 Marks

21) With the help of block diagram explain ASIC Design flow.
22) List and explain feature of CPLD.
23) Explain feature of FPGA.

4 Marks

24) With the help of internal block diagram, explain the architecture of Xilink family of CPLD.
25) Explain in details SPARTAN-3 Series.