

## Question Bank (G scheme)

Name of subject: DIGITAL TECHNIQUES

Unit Test: I

Subject Code: 17333

Courses: CM3G/IF

Semester: III

### CHAPTER 1: Introduction to Digital Techniques (16 marks)

#### 3 marks

- 1) Which are the advantages of digital circuits?
- 2) convert the following hexadecimal number into binary:  $(AFB2)_{16}$
- 3) Explain the following terms noise margin, power dissipation, propagation delay
- 4) Explain fan-out, fan-in and figures of merit
- 5) convert the following binary number to decimal number:  $(1011.01)_2$
- 6) Perform  $(9)_{10} - (4)_{10}$  using 1's complement method

#### 4 marks

- 7) Perform the following subtraction using 2's complement method:  
 $(11010)_2 - (10000)_2$
- 8) Write down the characteristics of CMOS.
- 9) Perform BCD addition for the following:
  - i)  $(85)_{10} + (39)_{10}$  or
  - ii)  $(368)_{10} + (427)_{10}$

### CHAPTER 2: Logic gates and Boolean algebra (18 marks)

#### 3 marks

- 1) Write down any six Boolean laws.
- 2) Explain principle of duality theorem.

#### 4 marks

- 3) Prove the following logic expression using Boolean algebra:

i)  $(A+B)(A+C)=A+BC$

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ii)  $A+AB=A+B$

4) Write down the truth table, logic symbol and Boolean expression for AND gate using 3 inputs.

5) Write down the truth table, logic symbol and Boolean expression for EX-OR gate using 2 inputs.

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ii)  $Y=AD+BCD+BCD$

6) Draw the equivalent circuit of the following gates using NAND gates

i) OR ii) AND

7) Draw logic circuit using universal gates for following logic equation:

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$Y = ABC + AC + BC$

8) Explain EX-OR Gate and EX-NOR Gate.

9) Simplify given expression and draw circuit diagram using only NOR Gate.

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$Y = ABC + BC + ABC + ABC$

10) Prove that

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$(A+B+C)(A+B+C)(A+B+C)(A+B+C) = A$

### CHAPTER 3: Combinational logic circuit. (26 Marks)

#### Mark 3:

1) Simplify Boolean expression.

$Y = \sum m(2, 4, 6)$

2) Draw half adder circuit using k map and realize it by using basic gates.

#### Mark 4:

3) Draw full adder circuit using k map and realize it by using basic gates.

4) Draw 4:1 mux. And give its truth table.

5) Implement 16:1 Mux using 4:1 Mux.

6) Implement the following expression using multiplexer  $Y = \sum m(0, 1, 2, 3, 6, 7)$ .