Question Bank (G scheme)

Name of subject: DIGITAL TECHNIQUES **Unit Test: II**

Subject Code: 17333 **Courses: CM3G/IF**

Semester: III

CHAPTER 3: Combinational Logic Circuit (26 marks)

3 marks:

1. What is K-map?

2. Design 4:1 MUX using 2:1 MUX

4 marks:

3. Explain Half Subtractor with logic implementation of gates.

4. convert the expression Y=AB+AC+BC into the canonical SOP form.

5. Simplify the following three variable Boolean expressions: Y=∑m (2, 4, 6)

6. Implement the following function using 8:1 MUX

Y=∑m(0,1,3,4,7).

CHAPTER 4: Sequential logic circuit (28 marks)

3 marks:

7. Explain J-K Flip Flop.

8. Explain 1-bit memory cell with working.

9. Draw the neat diagram of Master Slave J-K Flip Flop .

4 marks:

10. Draw the logical circuit diagram of clocked S-R Flip Flop using NAND gates. Description working.

11. Explain Race Around condition in J-K Flip Flop.

12. Draw the Block Diagram of sequential logic circuit and state the importance of clock signal.

13. Explain the triggering methods of Flip Flop.

14. Draw the neat diagram of Master Slave J-K FlipFlop .

15. Design clocked S-R Flip Flop with Preset and Clear.

16. Explain the significance of Preset and Clear in JK Flip Flop.

CHAPTER 5:A-D and D-A Converter(12 marks)

3 marks:

17. Give two Advantages and Dis-Advantages of ADC.

18. Compare Weighted Register DAC and R2R Ladder type DAC.

19.List any 4 applications of AD converter.

4 marks:

20. An 8 bit ADC has maximum voltage of 15V.What voltage change would each bit represent?

21. Classify the memories. What are the mechanism used for erasing EPROM?

22. Draw the Circuit Diagram of R-2R Ladder method of DAC.

23. Draw the block Diagram of Successive Approximation method of ADC.

24. Explain the Specifications of DAC.

25. Explain any 4 specifications of ADC.