Attempt any four of the following each carry 4 Marks:

Q 1] Realize the following expression using basic gates

$y = (A+ B).(AB)$ ii) y = A B + C +DE

Q 2] Perform binary multiplication of $(11001)_2$ X $(10011)_2$

Q 3] convert the following expression into standard SOP form?

1) y =AB + AC+ BC
2) y=X+XY+Y

Q 4] Compare TTL and CMOS and ECL logic families (any four points

Q 5] State and prove De-Morgan's First and second theorem for two variables

Q 6] Draw AND, gate using NAND gate only and NOR gate only

Q 7] Draw symbol, logical equation and truth table of 3 i/p AND gate and 3 i/p OR gates?

Q 8] Convert following octal into Hexadecimal

i) $(626)_8$

ii) $(1245)_8$

Q 9] Define min and max term.

Q 10] Write Boolean laws

Q11] Find 2's complement of:

i) $(110110)_2$ ii) $(010100)_2$

Q 12] Define power dissipation and figure of merit.

Q 13] Perform binary subtraction

i) $(101011)_2 - (10110)_2$ ii) $(11001)_2 - (10101)_2$

Attempt any four of the following each carry 3Marks:

Q 14] Write the symbol, Truth –table and logical expression of EX-NOR gate

Q 15] Simplify the Boolean expression given below

$Y=\Sigma m(1,3,5,9,11,13)$.

Q 16] Convert (78.5ABCD) into octal.

Q17] Convert (0.6875) into binary

Q18] Reduce the following expressions and implement using logic gates only.

$$Y=\bar{A}\bar{B}\bar{C}\bar{D}+\bar{A}BC\bar{D}+A\bar{B}CD+AB\bar{C}D$$

Q19] which are the advantages of digital circuits

Q20] Draw logic circuit using universal gates for following logic equation :

$$Y=\bar{A}BC+A\bar{C}+B\bar{C}$$

Q21] If $(396)_{10} = (A)_2 = (B)_{16}$, find A and B.

Q22] convert the expression Y=AB+AC+BC into the canonical SOP form.

Q23] Simplify the following three variable Boolean expression : Y=PiM(2,4,6)

Q24] Explain principle of duality theorm.

Q25] Perform BCD addition for the following:

i) $(85)_{10} + (39)_{10}$ or

ii) $(368)_{10} + (427)_{10}$

Attempt any four of the following each carry 4 Marks:

Q 1] Design Full Adder Circuit

Q 2] Draw the Logical block diagram of 4:1 MUX and describe its working using gates.

Q 3] Implement 1:32 DEMUX using 1:8 DEMUX.

Q 4] Draw the Block Diagram of BCD to SEVEN Segment Decoder with working.

Q 5] Implement the following function using 16:1 MUX
$Y=\sum m(0,1,3,4,7,12,15)$.

Q 6] Draw the logical circuit diagram of clocked S-R Flip Flop using NAND gates.Describe its working.

Q 7] Explain Race Around condition in J-K Flip Flop.

Q 8] Give two Advantages and Dis-Advantages of ADC.

Q 9] Draw the Circuit Diagram of R-2R Ladder method of DAC.

Q 10] Draw the block Diagram of Successive Approximation method of ADC.

Q11] Explain the Specifications of DAC.

Q 12] Draw the Block Diagram of sequential logic circuit and state the importance of clock signal.

Q 13] Explain the triggering methods of Flip Flop.

Attempt any four of the following each carry 3Marks:

Q 14] Design Half Adder Circuit

Q 15] Compare Weighted Register DAC and R2R Ladder type DAC.

Q 16]An 8 bit ADC has maximum voltage of 15V.What voltage change would each bit represent?

Q17] Classify the memories. What are the mechanism used for erasing EPROM?

Q18] Explain 1-bit memory cell with working.

Q19] Implement the following function using 8:1 MUX
$Y=\sum m(0,1,3,4,7)$.

Q20] Draw the neat diagram of Master Slave J-K Flip Flop .

Q21] Explain Half Subtractor with logic implementation of gates.

Q22] Design 4:1 MUX using 2:1 MUX

Q23] Explain J-K Flip Flop.

Q24]Design clocked S-R Flip Flop with Preset and Clear.

Q25] Explain the significance of Preset and Clear in JK Flip Flop.